

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

- 1 1. (Previously presented) A method for repairing defective memory
2 elements using self-test circuitry in a memory having a plurality of memory elements including a
3 first memory element and a second memory element, the method comprising:
4 counting fails in the first memory element with an on-chip logic counter;
5 counting fails in the second memory element with the on-chip logic counter;
6 comparing the number of fails in the first memory element to the number of fails
7 in the second memory element;
8 determining the one of the first memory element and the second memory element
9 having the most fails; and
10 allocating a redundant memory element to replace the one of the first memory
11 element and the second memory element having the most fails.
- 1 2. (Original) The method of claim 1 further comprising counting fails in
2 each additional memory element of the plurality of memory elements with the counter.
- 1 3. (Original) The method of claim 1 further comprising selectively
2 associating each one of the plurality of memory elements with the counter and counting the fails
3 in that memory element.
- 1 4. (Previously presented) The method of claim 2 wherein the memory
2 includes a plurality of redundant memory elements, the method comprising allocating each one
3 of the plurality of redundant memory elements to one of the plurality of memory elements
4 having the most fails.

1 5. (Original) The method of claim 4 wherein the memory is identified as
2 unrepairable when the number of memory elements having fails exceeds the number of
3 redundant memory elements.

1 6. (Previously presented) The method of claim 1 wherein the redundant
2 memory element replaces the first column or the second column only if one or more fails are
3 counted in the first column or the second column.

1 7. (Original) The method of claim 1 wherein the plurality of memory
2 elements include a plurality of columns and the redundant memory element includes a redundant
3 column.

1 8. (Original) The method of claim 1 wherein the plurality of memory
2 elements include a plurality of rows and the redundant memory element includes a redundant
3 row.

1 9. (Original) The method of claim 1 wherein the plurality of memory
2 elements includes a plurality of input/outputs and the redundant memory element includes a
3 redundant input/output.

1 10. (Original) The method of claim 2 wherein the memory further comprises
2 a second plurality of redundant memory elements perpendicular to the plurality of redundant
3 memory elements, the method comprising designating one of the memory elements as a must fix
4 memory element if a number of fails for that one of the memory elements exceeds a number of
5 the second plurality of redundant memory elements available for allocation.

1 11. (Original) The method of claim 10 wherein the plurality of redundant
2 memory elements includes columns and the second plurality of redundant memory elements
3 includes rows.

1 12. (Original) The method of claim 1 further comprising allocating a
2 perpendicular redundant memory element to repair any defects not repaired by the redundant
3 memory element.

1 13. (Previously presented) A method according to claim 1 wherein the
2 plurality of redundant memory elements include a plurality of columns and the redundant
3 memory element includes a redundant column, the method further comprising:
4 testing the redundant column to determine a number of failing bits;
5 determining if the redundant column has less fails than one of the plurality of
6 columns with the greatest number of failing bits; and
7 allocating the redundant column to replace the one of the plurality of columns
8 with the greatest number of failing bits if the redundant column has fewer failing bits.

1 14. (Original) The method of claim 1 wherein the steps of the method are
2 performed when power is applied to the memory.

1 15. (Currently amended) A computer program product embodied in a tangible
2 computer readable medium for repairing defective memory elements using self-test circuitry, the
3 defective memory elements in a memory having a plurality of memory elements including a first
4 memory element and a second memory element, the computer program product comprising:
5 computer executable code for counting fails in the first memory element with an
6 on-chip logic counter;
7 computer executable code for counting fails in the second memory element with
8 the on-chip logic counter;
9 computer executable code for comparing- the number of fails in the first memory
10 element to the number of fails in the second memory element;
11 computer executable code for determining the one of the first memory element
12 and the second memory element having the most fails; and

13 computer executable code for allocating a redundant memory element to replace
14 the one of the first memory element and the second memory element having the most fails.

1 16. (Previously presented) An apparatus comprising:
2 a memory having a plurality of memory elements;
3 a redundant memory element suitable for replacing at least one of the plurality of
4 memory elements;
5 a self-test circuit that tests the memory and allocates the redundant memory
6 element to one of the plurality of memory elements if a defect is found, the self-test circuit
7 including a multiplexer that selectively couples memory outputs to a fault counter that counts
8 fails in each one of the plurality of memory elements tested by the self-test circuit;
9 a compare circuit that compares the number of fails in each of the memory
10 elements and records the memory element having the most fails.

1 17. (Original) The apparatus of claim 16 further comprising a fault count
2 storage that stores numbers of fails and address information for one or more memory elements
3 containing fails detected during a self-test.

1 18. (Original) The apparatus of claim 16 wherein the plurality of memory
2 elements include at least one of a row, a column, or an input/output.

1 19. (Original) The apparatus of claim 16 further comprising a second fault
2 counter that counts fails in a second plurality of memory elements perpendicular to the plurality
3 of elements, the second fault counter selectively coupled to memory outputs by a multiplexer.

1 20. (Original) The apparatus of claim 16 further comprising a reset signal
2 provided to the fault counter after testing of each memory element.

1 21. (Original) The apparatus of claim 16 wherein the self-test circuit allocates
2 one or more redundant rows after allocating at least one of redundant columns or redundant
3 input/outputs.

1 22. (Original) The apparatus of claim 16, wherein the apparatus is provided
2 within an embedded memory of an integrated circuit.

1 23. (Currently amended) An apparatus for repairing a memory, the apparatus
2 comprising:
3 self-test circuitry for testing a plurality of memory elements, the self-test circuitry
4 including a multiplexer, fault detection circuitry, and count compare circuitry,
5 the multiplexer selectively coupling an output from one of the plurality of
6 memory elements to fault detection circuitry during a self-test, and
7 the count compare circuitry comparing the number of fails in each of the memory
8 elements and recording the memory element having the most fails.

1 24. (Original) The apparatus of claim 23 wherein the fault detection circuitry
2 includes an exclusive-or logic gate that compares a memory output to an expected memory
3 output.

1 25. (Original) The apparatus of claim 23 wherein the fault detection circuitry
2 includes a counter for counting fails within a memory element under test.

1 26. (Original) The apparatus of claim 25 wherein the self-test circuit provides
2 a reset signal to the counter after testing each one of the plurality of memory elements.

1 27. (Original) The apparatus of claim 23 wherein the fault detection circuitry
2 includes storage for storing fail data including a location of one of the memory elements and a
3 number of fails detected for the one of the memory elements.

1 28. (Original) The apparatus of claim 23 wherein fault data is provided to an
2 external device.

1 29. (Original) The apparatus of claim 28 wherein the fault data includes a full
2 bit fail map.